UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO, LTD; SAMSUNG ELECTRONICS AMERICA, INC.; SAMSUNG SEMICONDUCTOR INC., Defendants.	Case No. 2:22-cv-293-JRG JURY TRIAL DEMANDED (Lead Case)
NETLIST, INC., Plaintiff, vs. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; MICRON TECHNOLOGY TEXAS LLC, Defendants.	Case No. 2:22-cv-294-JRG JURY TRIAL DEMANDED

PLAINTIFF NETLIST INC.'S OPENING CLAIM CONSTRUCTION BRIEF

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I. The "rank" terms[1]

There are two areas of dispute. Netlist maintains that: (1) a "rank" cannot constitute a single memory device and (2) a "rank" of DDR memory devices corresponds to a fixed (i.e., non-variable) bit-width. That is particularly true for the '912 patent claims, which specify "memory modules" with "ranks" of "DDR memory devices." At the time of the '912 patent, and today, memory modules composed of DDR memory devices arranged in ranks are a standardized class of format defined by JEDEC specifications. The '215 and '417 patents are CIPs of the '912 patent, have a different disclosure, and do not specify "DDR memory devices" in the claims, but also include claims specifying "ranks" consistent with Netlist's proposed constructions.

A. "memory module . . . comprising," "first number of DDR memory devices arranged in a first number of ranks" and "second number of DDR memory devices in a second number of ranks" ('912 patent)

Netlist's Construction	Defendants' Construction
A "rank" of "DDR memory devices" is "a predetermined group of DDR memory devices on a memory module that can send or receive a fixed number of data bits via a fixed width data bus, in response to a read or write command and independently from other DDR memory devices on the memory module."	"rank" means "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module."

1. In the context of the '912 patent, a POSITA would not understand a single memory device to constitute a "rank."

The '912 patent claims recite a memory module comprised of "ranks" of double-data-rate ("DDR") memory devices. *E.g.*, Ex. 1 ('912), p. 45, 3:13-16 ("the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks"). "DDR" refers to a specific type of memory that is standardized by JEDEC. Ex. 4 (Stone Tr.), 21:20-22:12 ("There was a JEDEC standard by that date [2005] for DDR, yes."); Ex. 1 ('912), p. 28, 12:39-43 ("Table 3A

[1] All emphases are added unless otherwise indicated.

provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, 'Double Data Rate (DDR) SDRAM Specification,' published February 2004, and ***incorporated in its entirety by reference herein***."). The term "rank" is also a JEDEC-defined term. *See* Ex. 12 at 2 (Micron brand Crucial: "The term rank was created by JEDEC").

A POSITA at the time of the invention of the '912 patent reading the specification would have understood that a "rank" of "DDR memory devices" necessarily included more than one DDR memory device. The JEDEC standards in effect at the time provided for DDR memory devices having bit-widths of 4, 8, or 16 bits. Ex. 7 at 5 (DDR-1 standard JESD79 "defin[ing] the minimum set of requirements for JEDEC-compliant 64M **x4/x8/x16** DDR SDRAMs")[2]; Ex. 8 at 7-8 (DDR-2 standard JESD79-2 specifying **x4, x8, and x16** device configurations). Under Defendants' own construction, a "rank" of memory devices needs to read or write the "full bit-width of ***the memory module***." JEDEC-standard memory modules at the time of the invention were 64 or 72-bits wide. *See, e.g.*, Ex. 9 at 6 ("DIMM organization" "x72 ECC, x64"). To achieve the "full-bit-width" of a JEDEC-standard memory module—as required by Defendants' construction of "rank"—a POSITA would know that multiple 4-bit, 8-bit, or 16-bit DDR/DDR2 memory devices would be required, e.g., sixteen 4-bit devices, eight 8-bit devices, or four 16-bit devices per rank for a 64-bit wide memory module. Micron's expert Dr. Stone admitted that JEDEC standards defined DDR devices, that at the time of the invention modules of JEDEC-defined DDR devices were 64 or 72 bits wide, and as a result required multiple DDR memory devices in each rank:

> Q. JEDEC defines DDR memory devices; correct?
> A. That is correct.

Ex. 4 (Stone Tr.), 52:19-21.

[2] "x4" or "by four" refers to the bit-width of the memory device, in this case, four bits.

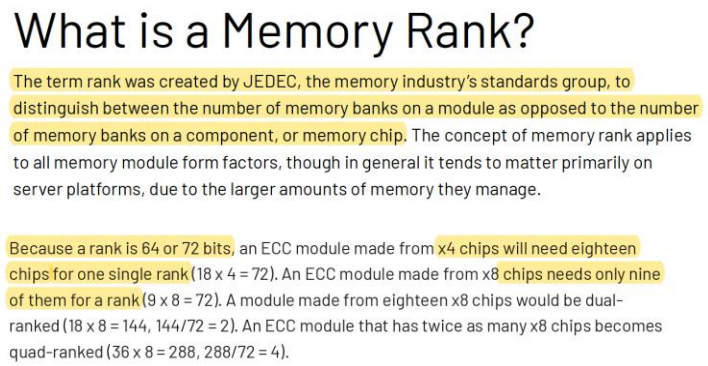
> Q. Once JEDEC was created and they began to specify . . . DDR memory devices, the width was either 64 or 72; correct?
> A. In the DDR and the DDR2 standards, the widths are 64 and 72, that is correct.
> Q. Okay. And for widths of 64 and 72 that, in the context of JEDEC DDR, a rank is always more than one chip?
> THE WITNESS: Again in the past ***it has been more than one chip*** and –

Id., 46:23-47:8 (objection omitted); *id.*, 45:9-19.

> Q. Why isn't it consistent?
> A. Ranks are -- I'm reading now to 2058. (As read): "Ranks are specific to memory modules and refer to a subarray made of multiple components."
> . . .
> Q. And so, in the present and past, rank has always been more than one chip?
> THE WITNESS: In the present and past for this definition of a rank, for this definition, it has been more than one chip.

Id., 43:6-11, 44:15-20 (objection omitted); *see also id.*, 48:1-3 ("Q. What does 64 and 72-bits wide mean -- mean to you in the context of DDR? A. Memory rank."), 48:25-49:4.

Dr. Stone admitted that "[a] POSA would believe that these patents were supposed to comply with JEDEC standards." Ex. 4 (Stone Tr.), 38:11-19; Ex. 5 (Stone Decl.), ¶ 44. Micron's documentation confirms that in JEDEC there is a specific definition of "rank" requiring more than one DDR memory device in each rank. *See* Ex. 12 at 2 (reproduced below).

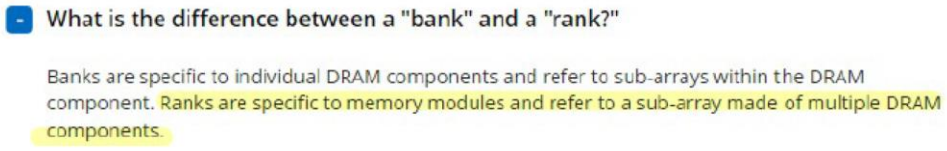


What is a Memory Rank?

The term rank was created by JEDEC, the memory industry's standards group, to distinguish between the number of memory banks on a module as opposed to the number of memory banks on a component, or memory chip. The concept of memory rank applies to all memory module form factors, though in general it tends to matter primarily on server platforms, due to the larger amounts of memory they manage.

Because a rank is 64 or 72 bits, an ECC module made from x4 chips will need eighteen chips for one single rank (18 x 4 = 72). An ECC module made from x8 chips needs only nine of them for a rank (9 x 8 = 72). A module made from eighteen x8 chips would be dual-ranked (18 x 8 = 144, 144/72 = 2). An ECC module that has twice as many x8 chips becomes quad-ranked (36 x 8 = 288, 288/72 = 4).

See also, e.g., Ex. 13 at 2-3:



What is the difference between a "bank" and a "rank?"

Banks are specific to individual DRAM components and refer to sub-arrays within the DRAM component. Ranks are specific to memory modules and refer to a sub-array made of multiple DRAM components.

In light of the JEDEC specifications in effect at the time of the patent, which require a rank of either 64 or 72 bits, in light of the fact that JEDEC specifications did not define DDR memory devices greater than 16 bits, and in light of the specific reference to "DDR memory devices" in the claim, a POSITA would understand that a "rank" of "DDR memory devices" would necessarily require more than one memory device in a rank.

The rest of the '912 patent specification supports this construction by repeatedly and consistently referring to "ranks" as ***multiple*** memory devices, e.g., with consistent references to plural "memory device***s***." Ex. 1 ('912), p. 28, 12:17-25 ("[I]n certain embodiments, two ranks of memory devices having a memory density are used to simulate ***a single rank of memory devices*** having twice the memory density…."); *id.*, p. 25, 6:31-38 ("[I]n certain embodiments, the memory device***s*** 30 are arranged in four ranks, as schematically illustrated by FIG. 1A. In other embodiments, the memory device***s*** 30 are arranged in two ranks, as schematically illustrated by FIG. 1B. Other numbers of ranks of the memory device***s*** 30 are also compatible with embodiments described herein."); *see also id.*, 7:55-8:43, 8:64-9:18 (logic tables "for the selection among ranks of memory device***s*** 30"); 2:16-17 ("The DRAM device**s** of a memory module are generally arranged as ranks or rows of memory . . . ."). The figures also consistently show multiple DDR memory devices in each rank. *See id.*, Fig. 1A-B, 2A, 3A (each rank 32, 34, 36 or 38 has multiple devices depicted). Indeed, the '912 patent specification does not describe a single embodiment with only one memory device per rank.

Netlist expects Defendants to argue that the '912 patent expressly contemplates single-device ranks based on the following: "In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of ***Table 1***). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time." Ex. 1 ('912), p. 26, 8:47-54. However, this passage is referring to sending a command signal to only one memory device in a "rank" with multiple memory devices. The embodiments

described with reference to Table 1 refer to transmitting a command signal to one of the multiple memory devices in the selected rank (i.e., one of at least two memory devices in the rank corresponding to CS_{1A}). This is because Table 1 is described as "a logic table compatible with certain embodiments described herein for the selection among ranks of ***memory devices [plural] 30*** using chip-select signals." *Id.*, 7:56-59. The "memory devices 30" are consistently described throughout the specification as part of multi-device ranks. *Id.*, 6:31-38; *see also* 20:64-65, 22:34-35; Figs. 1A, 1B, 2A, 3A.

The prosecution history of the '912 patent also supports Netlist's construction. During reexamination, the Examiner allowed claim 16 of the '912 patent by concluding that the Amidi reference failed to teach "transmit[ting] a command signal to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***." Ex. 10 at p. 3865-67. The Examiner thus construed a "rank" as comprising "a plurality of memory devices." The Requesters challenged the Examiner's interpretation and argued that claim 16 could cover embodiments where "'one memory device' encompasses a rank of [one] memory." *Id.* at p. 4442. The Board rejected that interpretation and upheld the Examiner's finding. Ex. 11 at pp. 79-80. The Federal Circuit confirmed the Board's findings. *Google LLC v. Netlist, Inc.*, 810 F. App'x 902 (Fed. Cir. 2020).

Finally, the extrinsic evidence supports Netlist's construction. In IPR2022-00063, Samsung asserted that "[t]he term 'rank' should be construed to mean an independent set of ***memory devices*** [plural] that act together in response to a memory command … to read or write the full bit-width of the memory module." Ex. 14 at p. 13. As another example, Samsung's corporate representative on the topic of JEDEC standardization of memory modules, confirmed that the text on p. 146 of Ex. 15 reflects a JEDEC proposal by Samsung. Ex. 16, 86:18-86:23.

Serial Presence Detect:

Byte 5 of the standard serial presence detect (SPD) describes the number of ranks of memory installed on the RDIMM. A rank of memory is defined as the collection of SDRAMs driven by a given rank select signal, S0 through S3. SPD byte 5 of a 4 rank RDIMM will contain the value 0x04.

Ex. 15 at p. 146. The witness, who was also the presenter, disagreed that a rank of memory could

include a single DRAM:

> Q: Sir, this statement is incorrect; the accepted definition of rank in 2007 or 2008 in the concept of DRAM memory modules includes a single DRAM; correct?
> A: ***No, that's not right***.

Ex. 16, 87:1-17 (objections omitted). That testimony comports with the JEDEC evidence discussed above.

In the IPRs filed by Samsung and Micron against the '912 patent, the PTAB tentatively construed "rank" as requiring one or more devices, but stated that it needed more briefing on the subject. Ex. 17 at 33 ("We do not view this issue as closed and will continue to consider any additional argument and evidence on this issue at trial."). The PTAB made this tentative decision without the benefit of Dr. Stone's admissions that in the specific context of DDR devices, a rank will involve more than one device. *Supra*, 2-3. The PTAB instead relied on an extrinsic treatise that was misinterpreted by both Samsung and Micron. Ex. 17 at 30-31 (analyzing Jacob, EX1033). Specifically, the Board observed that Jacob sets forth two potential definitions of the word "rank": "(1) a 'bank' of one or more DRAM devices that operate in lockstep in response to a given command"; and (2) "a set of DRAM devices that operate in lockstep to respond to a given command in a memory system." Ex. 18 at p. 413. However, Fig. 10.5 mentioned immediately before the first statement shows ***four*** devices per rank. *Id.*

10.2.2 Rank

Figure 10.5 shows a memory system populated with 2 ranks of DRAM devices. Essentially, a *rank* of memory is a *"bank"* of one or more DRAM devices that operate in lockstep in response to a given command. However, the word *bank* has already been used to describe the number of independent DRAM arrays within a DRAM device. To lessen the confusion associated with overloading the nomenclature, the word *rank* is now used to denote a set of DRAM devices that operate in lockstep to respond to a given command in a memory system.

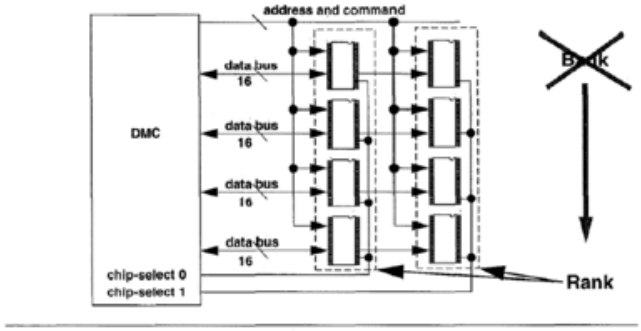


FIGURE 10.5: Memory system with 2 ranks of DRAM devices.

Jacob states that because "the word *bank* has already been used to describe the number of independent arrays within a DRAM device," the term "rank" is used "[t]o lessen the confusion." *Id.*

Hence, Jacob provides that "the word *rank* is ***now used*** to denote a set of DRAM devices that operate in lockstep to respond to a given command." *Id.* That is, it is the second statement that conveys the understanding of the term "rank" at the time of invention. That definition of "rank" mentions only "a set of DRAM device***s***," and hence ***excludes*** a single-device "rank." Jacob later notes that "a DRAM memory module can be organized as multiple ranks of DRAM devices on the same memory module, ***with each rank consisting of multiple DRAM devices***." *Id.* at p. 421; *see also id.* at p. 318 ("Each rank is ***a set of DRAM devices*** that operate in unison"); *id.* at p. 319 Fig. 7.5 ("Each rank is a set of ganged ***DRAM devices***").

Moreover, Jacob's reference to "operat[ing] in lockstep" would make no sense for a single-device rank because, in such a rank, there would be no other DRAM devices that operate "in lockstep" in response to a command. A single-device "rank" is also inconsistent with the rest of Defendants' construction that requires the memory devices in a rank "***act together*** in response to command signal" because "act[ing] together" again connotes multiple devices.

2. **"Ranks" are a pre-determined set of "DDR memory devices" that can output a fixed bit-width.**

The parties disagree about how a POSITA would determine which memory devices on a memory module belong to a particular "rank."

The claims of the '912 patent make clear which DDR memory devices comprise the "first number of DDR memory devices arranged in a first number of ranks" depends on the corresponding output signals. For example, claim 16 requires that the "set of output signals" generated by the memory module circuit are "configured to control the first number of DDR memory devices arranged in the first number of ranks." Ex. 1 ('912), p. 44, 3:13-16, 3:29-31. A POSITA would understand that a chip-select signal is configured to control ranks of DDR memory devices, e.g., by selecting or activating a rank during operations. *See id.*, p. 23, 2:35-38. For example, Table 1 provides a logic table

with states indicating when the rank corresponding to each chip-select signal is selected. *Id.*, p. 27-28, 8:55-9:18; 9:19-43 (describing states where specific ranks are selected based on which chip-select values are "low," or active). In Fig. 1A, each rank of memory devices has its own dedicated chip-select signal lines (e.g., a rank corresponding to CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}). A POSITA would understand that "chip-select signals" are used for selecting ranks for operations such as read or write. Ex. 8 at 6 ("CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code."). Thus, each "rank" of DDR memory devices is associated with a unique chip-select signal and is, in that sense, a "pre-determined" group of memory devices.

The specification teaches that "[t]he DRAM devices of a memory module are generally arranged as ranks or rows of memory." Ex. 1 ('912), p. 23, 2:16-18. Defendants' construction would require a "rank" to "read or write the ***full bit-width*** of the memory module." If the full bit-width of the memory module was not fixed, that would mean that the number of devices in a purported "rank" could change as the "full bit-width of the memory module" changes. Nothing in the '912 patent suggests, however, that a rank of memory devices refers to a group of memory devices that is dynamically reconstituted to account for the changing memory bit width. To the contrary, Fig. 1A shows four ranks mounted on a printed circuit board, each rank with its corresponding CS. *E.g.*, *id.*, p. 25, 6:31-38; *see also* Figs. 4A-4B, 5C-5D, 8A-8D, 9A-9B, 10A-10B, 11A-11B. Nor does anything in the JEDEC standards suggest that a "rank" of memory devices can dynamically change. Indeed, JEDEC standards at the time indicate that each "rank" is associated with its own chip-select signal and outputs or receives data via a fixed width data bus such as 64-bit wide or 72-bit wide. Ex. 9 at 12.

The testimony of Micron's claim construction expert is on point. Dr. Stone testified that 64 or 72 bits in the context of DDR is the width of a memory rank. *See* Ex. 4 (Stone Tr.), 48:1-3 ("Q. What does 64 and 72-bits wide mean -- mean to you in the context of DDR? A. Memory rank."). Ex. 9 at 5 (JEDEC DDR RDIMM standard specifying fixed 64 or 72-bit width modules), Ex. 19 at 6

(JEDEC SODIMM standard specifying fixed 64 or 72-bit width modules).

B. The use of the term "can" in the phrase "can send or receive" reflects an important part of the inventions.

As discussed above, a "rank" of memory devices can send or receive the full bit-width of the module (e.g., 64 or 72 bits) in response to read or write commands. *Supra*, 7-8. But nothing in the asserted patents requires that all the memory devices in one rank simultaneously send or receive data under all circumstances. In other words, the asserted patents contemplate "ranks" of memory devices where a subset of memory devices (e.g., only one memory device) sends or receives data at a time. *See, e.g.*, Ex. 1 ('912), p. 45, cl. 16. The specification teaches that "[d]uring operations the ranks of a memory module are selected or activated by control signals that are received from the processor." *Id.*, p. 23, 2:35-37. It also provides a specific example where, in a multi-device rank, "data is supplied from one memory device at a time." Ex. 1 ('912), p. 26, 8:47-54; Ex. 2 ('215), 19:14-19; Ex. 3 ('417), 19:14-19; *supra*, 4-5 (explaining that '912, 8:47-54 is directed to multi-device ranks). Put differently, a POSITA would understand that a "rank" must have the capability to send or receive the full bit-width of the memory module, but need not always do so.

Testimony from Samsung's IPR expert Dr. Wolfe supports Netlist's construction. Dr. Wolfe testified that one would still call something a "rank" if it had the capability to partially output the full bit-width of the module. Ex. 31, 36:2-10 ("Q. I thought a rank is a collection of DRAMs that respond to a common memory command simultaneously. That's not your understanding of what rank is? THE WITNESS: That is my understanding. But I think in common usage, ***one would still call something a rank if it had that capability but also had the capability to do a partial read***." (objection omitted)), 37:8-14 ("A rank of memory in the way that we ordinarily use that term is capable of providing an output on a read from every memory die or every memory element in the rank simultaneously, but ***we would still in normal usage still call it a rank if it also had the capability***

of only providing a portion of the memory word.").

C. "memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks" ('417 patent)

Netlist's Construction	Defendants' Construction
"a predetermined group of memory devices on a memory module that can send or receive a fixed number of data bits via a fixed width data bus, in response to a read or write command and independently from other memory devices on the memory module"	"rank" means "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module."

The term "rank" in the context of the '417 patent should likewise not be construed to encompass a single memory device. First, the claim language expressly requires multiple memory devices in each rank. Ex. 3 ('417), 42:41-47. Dr. Stone admits that the '417 patent requires JEDEC-compliant memory modules. Ex. 4 (Stone Tr.), 38:2-39:8 (for the patents-at-issue "A POSA would believe that these patents were supposed to comply with JEDEC standards"); Ex. 5 (Stone Decl.), ¶ 44. For the reasons explained above, a POSITA would understand a JEDEC-compliant memory module would require ranks that each comprise more than one memory device. *Supra*, 1-7.

Additionally, the term "rank" in the context of the '417 patent should be construed to require a predetermined group of memory devices that can output a fixed bit width. The claims of the '417 patent make clear that which devices constitute a "rank" depends on the corresponding chip-select signals that control those devices. For example, claim 1 of the '417 patent requires:

> memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, ***wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals . . .wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value*** and the other registered address and control signals ***is configured to receive or output a burst of N-bit wide data signals in response to the read or write command*** . . . .

Ex. 3 ('417), 42:41-54. The rank of "memory devices" that receives a chip-select signal having the "active signal value" is configured to output N-bit wide data signals. Thus, the "ranks" of memory

devices would be organized in a predetermined group and have a fixed bit-width. *Supra*, 7-10.

D. "plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank" ('215 patent)

Netlist's Construction	Defendants' Construction
"a predetermined group of memory integrated circuits on a memory module that can send or receive a fixed number of data bits via a fixed width data bus, in response to a read or write command and independently from other memory integrated circuits on the memory module"	"rank" means "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module."

The term "rank" in the context of the '215 patent should also not be construed to encompass a single memory integrated circuit ("IC"). Dr. Stone admits that the '215 patent requires JEDEC-compliant memory modules. Ex. 4 (Stone Tr.), 38:2-39:8 ("A POSA would believe that these patents were supposed to comply with JEDEC standards"); Ex. 5 (Stone Decl.), ¶ 44. A POSITA would understand a JEDEC-compliant memory module would require ranks of memory integrated circuits that each comprise more than one memory integrated circuit. *Supra*, 1-7.

Claim 1 of the '215 patent recites, among other things:

> a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank

Ex. 2 ('215), 37:35-38; 3:32-35. In context, this claim language supports subsequent requirements of a buffer and logic that can control at least one memory device in the first and second rank. *See id.*, 37:46-50 ("a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus"), 37:51-62 ("logic coupled to the buffer"). It is not saying that the first and second rank can only have one memory device in them. The specification is in accord. *See, e.g.*, *id.*, 3:44-61 (describing a "buffer coupled between the at least one first memory integrated circuit and the memory bus," as well as "logic"

configured to provide "control signals to the buffer to enable communication . . . between the at least one first memory integrated circuit and the memory controller through the buffer").

Additionally, the term "rank" in the context of the '215 patent should be construed to require a predetermined group of memory devices that can output a fixed bit width. The claims of the '215 patent make clear that which devices constitute a "rank" depends on the chip-select signals that control those devices. For example, claim 1 of the '215 patent requires that "the first rank is selected to receive or output the first data burst in response to the first memory command." Ex. 2 ('215), 37:32-50. As noted above, chip-select signals are used to select or activate a rank for operation. *Supra*, 1-9. A POSITA would thus understand that the "ranks" of memory devices would be organized in a predetermined group and have a fixed bit-width. *Id.*

II. "signal" / "row[/column] address signal" ('912, all claims)

The claims of the '912 patent require certain components to receive input "signals" from the computer system, with modifiers describing the type of signals to be received, for example, a "row address" signal or a "column address" signal. *E.g.*, Ex. 1, p. 43, 1:34-38 (claim 1: logic element receives "a set of input control signals . . . comprising at least one row/column address signal, bank address signals, and at least one chip-select signal"). Defendants, relying on a 15-year-old, agreed-to construction of the term "signal" from previous litigation involving the '912 patent, apparently intend to argue that "signal" should be broadly construed to encompass packetized control and address information to the memory module that is then decoded by on-module logic into discrete output signals. In the N.D. Cal. litigation involving the '912 patent, Netlist agreed that the term "signal" means "a varying electrical impulse that conveys information from one point to another." Ex. 21 at 7. There was no discussion in the 15-year-old construction of the "packetized" theory.

The claims of the '912 patent recite a memory module that receives discrete control and address "signals," not packetized information. As Fig 1A of the '912 patent shows, each type of signal

is associated with its own discrete line, e.g., a chip-select line for input chip-select signals. *See also* Ex. 1 ('912), p. 8-9, Figs. 2A, 3A. No construction is needed for the jury to understand what a "signal" is, nor what a "row address" or "column address" signal is. The '912 specification also consistently refers to "signals" as discrete, non-packetized types:

> As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. . . .
>
> The memory module 10 receives row/column address signals or signal bits (A_0-A_{n+1}), ***bank address signals*** (BA_0-BA_m), ***chip-select signals*** (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n ***row/column address signals*** are received by the register 60, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices 30. The logic element 40 receives the two ***chip-select signals*** (CS_0, CS_1) and one ***row/column address signal*** (A_{n+1}) from the computer system. Both the logic element 40 and the register 60 receive the ***bank address signals*** (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Ex. 1 ('912), p. 25, 7:39-53, p. 24, 6:55-63; *see also id.* Table 1 and 8:19-43 (description of Logical States based on values asserted on CS_0, CS_1, A_{n+1}, and Command lines).

Micron's expert claims that "[a] POSA would believe that these patents were supposed to comply with JEDEC standards." Ex. 4 (Stone Tr.) 38:2-39:8. The claims are limited to "DDR" memory devices, which refers to "double-data rate," a type of memory standardized by JEDEC. *See, e.g.*, Ex. 1 ('912), p. 28, 12:38-44 (incorporating by reference JEDEC DDR standard); Ex. 5 (Stone Decl.), ¶ 44; *supra* at 2-3. In JEDEC, each bus "is dedicated to handle only its designated function." Samsung's expert Dr. Wolfe agreed that the JEDEC standards do not feature packetized control and address input signals. Ex 22, 28:8-16 ("Q. And in the – in the traditional DIMM, is the multiplex control and address information demuxed from the data? . . . . No, not in a traditional DIMM that it would be compliant with JEDEC Standard 21-C [Ex. 9]. It would not have that characteristic.").

III. "in response" ('912, claims 1, 15, 28, 39, 77, 80, 82, 86, 88, 90)

Amended claim 1 of the '912 patent is representative of the parties' dispute. Claim 1 requires a memory module comprising a circuit with a "logic element," wherein:

> the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal.

Ex. 1 ('912), p. 44, 2:11-18. The defendants would like to insert "all four of" before the enumerated signals. During meet and confer, counsel for Defendants suggested that the "in response" terms require the logic to "use" all four input signals as inputs to logic equations used to generate the output signals. There is no basis in the intrinsic record for such a limitation.

The claims simply require that the "logic element" generate output CAS or chip-select ("CS") signals "in response, at least in part" to the enumerated input signals. The claims do not require and the specification does not suggest that all four signals must be "used" to generate the output CAS or CS signals, as Defendants apparently interpret. For example, in Table 4, the first and third rows show examples where the logic element generates chip-select signals "in response" to bank address signals (signal ii), even though the bank address signals are not used as the density transition bits in the translation logic. Likewise, the second row shows an example where the translation logic equation uses bank address signals, but not row address signals. Ex. 1 ('912), p. 28, 12:66-13:25 (Table 4 lists density transition bits for memory device transitions listed in 3B), 12:29-32 (logic element 40 of "utilizes implied translation logic equations having variations ***depending on*** whether the density transition bit is a row, column, ***or*** internal bank address bit"). Furthermore, the claims do not require the enumerated signals to necessarily be inputs to translation logic equations. For example, the input signal (e.g., the clock signal) may affect the timing

TABLE 4

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	to be determined

Same Number of Internal Banks

Bank Address Signal is Not Used

of the output signal generation, resulting in the output signal being in response to the recited signal.

IV. "A memory module connectable to a computer system, the memory module comprising" ('912, preamble to all asserted claims)

The preamble of the '912 claims is limiting. "[A] preamble limits the invention if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). In *Samsung I*, the Court found that the preamble ("a memory module") of similar claims was limiting because "a skilled artisan would understand a 'memory module' is distinct from, and has essential structural requirements not necessarily found in, other modular computer accessories," including structure necessary to connect to a memory controller. Ex. 6 at 29. The '912 specification emphasizes that the memory module is connectable in a computer system to a memory controller. Ex. 1 ('912), p. 28, 11:43-47, p. 32, 19:67-20:56, p. 33, 22:22-24; Figs. 1A/1B, 2A, 3A (depicting signal lines from memory controller). Samsung's expert in the '912 IPR testified that at the time of the invention a "memory module" would have been understood to go into a "dedicated memory slot in a computer system and not a general-purpose IO slot," as distinct from other modular components such as a PCI card. Ex. 22, 100:22-101:8.[3]

V. "logic" ('417, claim 1; '215, claims 1 and 21)

A. The "logic" terms are not subject to § 112, ¶ 6.

Micron contends that the "logic" limitations of '215 claim 1 and '417 claim 1 are subject to § 112, ¶ 6. Ex. 5 (Stone Decl.), ¶ 32. The relevant claim language is reproduced below.

> '215 claim 1: **logic** . . . configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the **logic** is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer.

[3] For similar reasons, the preamble of the '608 patent is limiting. *See* Ex. 32, 19:14-18.

> '417, claim 1: **logic** . . . configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, . . . the **logic** is further configurable to output data buffer control signals in response to the read or write memory command.

The "logic" terms, which do not use "means," are not subject to § 112, ¶ 6. "[T]he failure to use the word 'means' . . . creates a rebuttable presumption . . . that § 112, para. 6 does not apply." *Williamson v. Citrix Online LLC*, 792 F.3d 1339, 1348-49 (Fed. Cir. 2015) (*en banc*). "In the absence of the word 'means,'" Micron bears the burden of demonstrating "by a preponderance of the evidence that the ['logic' limitation] fails to recite sufficiently definite structure." *Dyfan, LLC v. Target Corp.*, 28 F.4th 1360, 1370-71 (Fed. Cir. 2022). Micron cannot meet that burden here.

Courts in this district have repeatedly "concluded that in many instances the word 'logic,' like 'circuit' or 'processor,' may connote sufficiently definite structure and is not a "nonce" or "functional" word that is subject to the limitations of § 112 ¶ 6." *CDN Innovations, LLC v. Grande Commc'ns Networks, LLC*, 2021 WL 3615908, at *11 (E.D. Tex. Aug. 13, 2021) (collecting cases); *CA, Inc. v. Netflix, Inc.*, 2021 WL 5323413, at *21 (E.D. Tex. Nov. 16, 2021); *Sonrai Memory Ltd. v. Oracle Corp.*, 2022 WL 800730, at *9 (W.D. Tex. Mar. 16, 2022) (Yeakel, J.) (finding that "logic" in the context of computer memory patents provided sufficient structural meaning in light of the claims and specification and distinguishing *Egenera, Inc. v. Cisco Sys.*, Inc., 972 F.3d 1367 (Fed. Cir. 2020), on that basis).

Here, the specifications of the '215 and '417 patents make clear that the term "logic," as used in the claims of those patents, is not a nonce term. For example, the specifications teach that a logic element may be "selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD)" or may be "a custom device." Ex. 2 ('215), 6:36-48; Ex. 3 ('417), 9:54-10:4. Micron's expert Dr. Stone admits that POSITAs would be familiar with the structure and operation of logic elements like ASICs and CPLDs.

See Ex. 5 (Stone Decl.), ¶ 21 (POSITA would have been familiar with "have been familiar with the ***structure*** and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs."). Dr. Stone confirmed at deposition that "logic" has structure, e.g., transistors. Ex. 4 (Stone Tr.), 9:3-8 ("[Q.] You understand that logic has gates, sometimes referred to as transistors, AND, OR, XOR, NOT, NAND, NOR, and XNOR? A. I am familiar -- 09:08 THE WITNESS: Okay. I am familiar with this." (objection omitted)). Dr. Stone also admitted that "[l]ogic includes circuitry with state and circuitry without state," and that "circuitry with state and circuitry without state" are "*actual structures*." *Id.*, 16:25-17:14 ("[Q.] Logic includes circuitry with state and circuitry -- circuity without state? A. Yes. Logic -- computer logic[] may have state and may not have state. Q. And circuitry with state and circuitry without state, those are actual structures; right? You can go to textbooks and look those up. Those are actual structures." (objections omitted)). Dr. Stone also defined "computer logic" as "circuitry that performs Boolean operation." *Id.*, 11:6-22; *see also id.*, 10:17-21 ("Logic circuitry is circuitry that performs a Boolean logic."). He also confirmed that he could examine a circuit and determine if it was logic. *Id.*, 17:21-18:3 ("[Q.] I'm asking it in the opposite way, which is that, you can go and look and physically see if the circuitry is logical circuitry; circuitry with state and circuitry without state? A. I can. If -- if I have all of the information available to me, I can make that determination."). And Micron's co-defendant Samsung does not contend that the "logic" terms lack structure. *See* Dkt. 94-2 at 19-20, 33-34.

The patents also teach that "[i]n certain embodiments, the PLD 42 use sequential and combinatorial logic procedures …." Ex. 2 ('215), 29:61-30:3. Samsung's IPR expert, Dr. Wolfe, agreed that a POSITA would have been familiar with sequential and combinatorial logics. Ex. 22, 117:8-119:18 (noting e.g., "sequential logic" "describes a combination of logic functions and registers," "combinatorial logic" generally refers to logic without storage units and without requiring clock).

Finally, even if the court determines that the "logic" terms are subject to § 112, ¶ 6, the terms

are not indefinite because the specification discloses sufficient structure for performing the claimed function. *See, e.g.*, Ex. 3 ('417), 3:50-52, 4:1-6, 4:23-29, 7:17-31 (logic is PLD, ASIC, FPGA, or CPLD), 7:32-35, 9:37-10:4, 15:33-40, 16:36-59, 17:6-9, 17:65-18:3, 22:49-56, 34:34-44, Figs. 5A-5D, 9A-9B, Verilog examples 1-3 (describing physical hardware structures that perform logic functions). Micron's expert Dr. Stone contends that the claims are indefinite because there is no corresponding disclosure of logic providing control signals to the data buffer. Ex. 5, ¶ 37 (asserting specification does not disclose structure for logic "providing [] control signals to the buffer to enable communication of the [] data burst" of '215 claim 1), ¶ 40 (similar argument for '417 claim 1). Contrary to Dr. Stone's assertion, the specification discloses structure for performing this function. *See e.g.*, Ex. 3 ('417), 7:32-35 ("In certain embodiments, the circuit 40 further comprises one or more switches which are operatively coupled to the ***logic element to receive control signals*** from the logic element."); 7:17-31 (logic is PLD, ASIC, FPGA, or CPLD), 9:37-10:4, 34:34-44.

B. The "logic" terms are not limited to "fork-in-the-road."

Samsung contends that the "logic" terms of '215 claims 1 and 21 are subject to what the parties have previously referred to as a "fork-in-the-road," where one data signal line between the buffer and the first rank of memory ICs is enabled (i.e., along a first "prong" of the "fork") while a second data signal line between the buffer and the second rank of memory ICs is disabled (i.e., along a second "prong" of the "fork"):

Term	**Samsung**
"logic coupled to the buffer and configured to respond to the **first memory command** by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer";	"logic coupled to the buffer and configured to respond to the **first memory command** by providing first control signals **to selectively electrically couple the input of the buffer to a first data signal line at the output of the data buffer** to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, **and disabling a second data signal line at the output of the buffer connected to**

('215, claim 1)	**the second memory integrated circuit**"
"wherein the logic is further configured to respond to the **second memory command** by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals"; and ('215, claim 1)	"wherein logic is further configured to respond to the **second memory command** by providing second control signals to **selectively electrically couple the input of the buffer to a second data signal line at the output of the data buffer** to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, **and disabling a first data signal line at the output of the buffer connected to the first memory integrated circuit**"

Should the inventors have desired to import such limitations from the specification, they would have done so. For example, U.S. 9,037,774 in the same family recites isolating one set of DQ and DQS signals when another set is being used for receiving or outputting data. *E.g.*, Ex. 28 ('774 patent), 42:5-8 ("circuit . . . ***isolates*** the second set of module DQ and DQS signal lines from the data bus as the memory module is receiving or outputting the first data burst"). The '215 and '417 patents do not impose such "isolat[ion]" requirements. And because the claims impose no such requirements, Samsung's evidence is also inapposite because it involves ***different*** patents that use ***different*** claim language such as "selectively coupling" or "selectively isolating." Ex. 24 ('150 patent), 41:40-43 (cl. 1: "wherein the circuit is configurable to be responsive to the set of input signals by ***selectively isolating*** one or more loads of the DDR memory devices from the computer system"); 42:58-63 (cl. 15 "selectively electrically coupling"); 43:51-54 (cl. 22); 44:46-50 (cl. 31); Ex. 25 ('536 patent), 41:28-39 (cl. 1: "the circuit including at least one configuration in which the circuit is configured to . . .

selectively isolate a load of the DDR memory circuits of at least one rank of the first number of ranks from the computer system in response at least in part to the set of signals"); 43:33-36 (cl. 24); 44:56-60 (cl. 38). The claims of the '215 patent, by contrast, do not use the "selectively coupling" or "selectively isolating" language. Samsung's attempt to redraft the claims should be rejected, and the evidence it relies upon actually supports Netlist's position—i.e., the patentee knew how to claim the "fork-in-the-road" arrangement and chose not to do so here.

Claim 1 of the '215 patent is clear that the first memory integrated circuit in the first rank is selected to receive or output a first data burst in response to the first memory command, and that the second rank is not selected to receive or output data in response to the first memory command. But not selecting one rank to receive or output data is not the same as disabling a data signal line. The "logic" limitation simply provides further detail regarding how the data is transmitted through the data buffer to the selected rank of memory devices, i.e., by using on-buffer logic that provides control signals to the buffer to "enable communication" of the first data burst in response to the first memory command, or the second data burst in response to the second memory command. Ex. 2 ('215), 37:31-62.

The specification likewise explains that the on-buffer logic provides control signals to the buffer to "enable communication" in response to a first or second memory command, with no requirement that the data path for the non-selected rank be disabled. Ex. 2 ('215), Abstract, 3:44-61. While certain embodiments describe load isolation through "selectively coupling"/"selective isolation" of the memory devices from the memory controller, those features are ***not*** claimed here. Nor are those the only embodiments. Figs. 8A and 8B, for example, do not have switches that isolate the DQ lines of rank a and rank b, which are both connected to the same common DQ signal line 112, and thus is not a "fork-in-the-road" arrangement. *See id.*, Figs. 8A-8B. A claim construction that excludes preferred embodiments is "rarely, if ever, correct." *Kaufman v. Microsoft Corp.*, 34 F.4th 1360,

1372 (Fed. Cir. 2022).

VI. "circuitry" ('417, claims 1, 6, 11)

A. The "circuitry" terms are not subject to § 112, ¶ 6.

Micron contends that certain limitations that recite "circuitry" are subject to § 112, ¶ 6:

1) "**circuitry** . . . configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals" (**'417, cl.1**);

2) "**circuitry** includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the **circuitry**" (**'417, cl. 6**);

3) "**circuitry** is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths" (**'417, cl. 11**).

Ex. 5 (Stone Decl.), ¶ 52. Micron also contends the terms are indefinite because there is no corresponding structure in the specification. *Id.*, ¶¶ 55-57. Micron's arguments should be rejected.

First, "circuitry" is not a nonce term. The Federal Circuit has "previously held on several occasions that the term 'circuit' connotes structure" such that § 112, ¶ 6 does not apply. *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 711 F.3d 1348, 1364-65 (Fed. Cir. 2013) (citing *MIT v. Abacus Software*, 462 F.3d 1344, 1355 (Fed. Cir. 2006), *Linear Tech. Corp. v. Impala Linear Corp.*, 379 F.3d 1311, 1320-21 (Fed. Cir. 2004), and *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1373 (Fed. Cir. 2003)). For example, in *Apex*, the Federal Circuit concluded that the term "circuit" recited sufficient structure in the context of the claims at issue. 325 F.3d at 1372-73 (considering the use of the term "circuit" in the claim limitation "a first interface circuit for receiving keyboard and cursor control device signals from the workstation"). The court observed that "the term 'circuit' with an appropriate identifier such as 'interface,' 'programming' and 'logic,' certainly identifies some structural meaning to one of ordinary skill in the art." *Id.*

Here too, the claims identify "circuitry" with certain structural meaning to one of ordinary skill in the art—i.e., a combination of a number of electrical devices and other components that can

be interconnected to transmit data. For example, claim 1 describes circuitry "***coupled between*** the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks. . . ." Ex. 3 ('417), 42:54-57. Claim 6 identifies "circuity" that "***includes logic pipelines*** configurable to enable the data transfers ***between the memory devices*** and the ***memory bus through the circuitry***." *Id.* at 43:19-22. Claim 11 identifies "circuitry" that "***includes data paths***" and modifies the circuitry to be "configurable to enable the data paths in response to the data buffer control signals . . . ." *Id.* at 44:9-14. Thus, section 112, ¶ 6 does not apply where, as here, "the structure-connoting term [circuitry] is coupled with a description of the circuit's operation." *Linear Tech.*, 379 F.3d at 1320 (claim reciting "a first circuit for monitoring a signal from the output terminal to generate a first feedback signal" did not require § 112, ¶ 6 treatment because "[t]he contextual language describes the objective of the 'circuit' . . . and the desired output of the 'circuit'"); *see also Estech Sys., Inc. v. Target Corp.*, 2021 WL 1090747, at *24 (E.D. Tex. Mar. 21, 2021). ("Like the claim-recited 'detector' in *Personalized Media* and the claim-recited 'circuit' in *Linear Technology*, the 'circuitry' terms here provide sufficiently definite structure to maintain the presumption against § 112, ¶ 6. Notably, the term 'circuitry' itself connotes a broad class of structures.").

Extrinsic evidence supports Netlist's position. The word "circuit" or "circuity" is a well-known term in electronics that connotes structure, such as an "[a]rrangement of conductors and passive and active components forming a path, or paths, for electrical current." Ex. 29 (Chambers Dictionary of Science and Technology, 2007) at 224. Other contemporaneous dictionary definitions are in accord. *See, e.g.*, Ex. 30 (Comprehensive Dictionary of Electrical Engineering, 2005) at 4 (defining "circuit" as "a ***physical device*** consisting of an interconnection of elements . . . . For example, an electric circuit may be constructed by interconnecting a resistor and a capacitor to a voltage source."); Ex. 20 (Dictionary of Computing, 2008) at 3 (defining "circuit" as "[t]he combination of a number of electrical devices and conductors that, when interconnected to form a conducting path, fulfill some

desired function"). Micron's expert Dr. Stone does not cite any of these well-known definitions, so his testimony should be afforded little weight. Ex. 5 (Stone Decl.), ¶¶ 50-57. In fact, Micron's expert Dr. Stone previously testified that a "circuit" is "a collection of electrical components connected together in some fashion," Ex. 23, 23:9-17, which requires structure. And Micron's co-defendant Samsung does not contend that the "circuitry" terms lack structure. *See* Dkt. 94-2 at 15-19.

Even if subject to § 112, ¶ 6, the "circuitry" terms are not indefinite because the specification discloses sufficient corresponding structure. For example, with respect to the circuitry for transferring data bursts, the patents provide corresponding structures in Figs. 3A-3B, 4A-4B, 5A-5D, 8A-8D and their accompanying descriptions, as well as Verilog code example 1. *See, e.g.*, Ex. 3 ('417), 8:10-10:4 (describing structural features of buffer circuitry illustrated by Figs 3A-5D); 10:58-13:23 (Verilog code example defining physical hardware structures that provide load isolation to DQ and DQS lines); 14:37-15:61 (describing structural features of buffer circuitry illustrated by Figs. 8A-8D, including potential use of FET switches or multiplexers). Similarly, with respect to circuitry providing logic pipelines, the patents provide corresponding structures such as ASIC, PLD, CPLD, FPGA, sequential and combinatorial logics. *See*, *e.g.*, *id.*, 9:37-10:4. Thus, contrary to Dr. Stone's assertions, the '417 specification describes corresponding structure for the circuitry limitations. *See* Ex. 5 (Stone Decl.), ¶ 55. Thus, even if "circuitry" is construed as a 112, ¶ 6 term, the claims encompass those disclosed structures and their equivalents.

B. Samsung's construction of "circuitry" should be rejected.

Samsung, while not contending the "circuitry" limitations are subject to § 112, ¶ 6, would construe the terms to introduce the "fork-in-the-road" concept explained above. Samsung's construction would improperly import 60+ words into the plain language of claim 1:

Term	Samsung
"circuitry coupled between the data	"**a data buffer** coupled between the data signal lines in

signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals"	the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, **the buffer configurable to selectively electrically couple a single data signal line at the input of the buffer to a first signal line and second signal line at the output of the buffer** to transfer N-bit wide data signals between the N-bit wide memory bus and the memory devices **in the one of the plurality of N-bit wide rank, wherein each signal line at the output of the buffer is connected to a different N-bit wide rank**."

The plain language of the claims does not require the first rank and second rank of memory integrated circuits to be on different "forks," as Samsung's construction contemplates. Furthermore, as discussed with respect to "logic," the specification includes ***unclaimed*** embodiments with a "fork-in-the-road" configuration, but those embodiments are only exemplary. *Supra*, 18-20. Nor does the prosecution history or any extrinsic evidence necessitate the court import aspects of those example embodiments into the claims, as Samsung attempts to do.

VII. "the at least one of the circuit components" ('215, claim 15)

Netlist and Samsung agree that this term should be given its plain and ordinary meaning. Dkt. 94-1 at 73; Dkt. 94-2 at 43. Micron contends that the term is indefinite, apparently for lack of antecedent basis. Dkt. 94-3 at 53. The term "the at least one of the circuit components" is not indefinite because it refers to the "circuit components" of buffers disclosed in claim 14, which claim 15 depends on. *See* Ex. 2 ('215), 39:24-33. The plain language of claim 14 requires that the "circuit components" be configurable to provide a "first data path" or a "second data path," and claim 15 further requires that the "circuit components" do so in response to "first[/second] control signals." The fact that claim 15 uses "at least one" to refer to the "circuit components" is of no moment, since the recitation of "circuit components" in claim 14 is the only reference to that term in the dependency chain. *Gree, Inc. v. Supercell Oy*, 2020 WL 2332144, *34 (E.D. Tex. May 11, 2020) (rejecting indefiniteness argument for lack of antecedent basis where claim 1 recited "***the*** frame" and dependent claim 2

required "the display to move ***first*** frame" because "there is only one frame in the dependency chain and there is only one frame for which a slide operation is identified").

VIII. "burst of data strobe signals" ('215, claims 12, 13, 28, 29)

Netlist and Samsung agree that "burst of data strobe signals" should be given its plain and ordinary meaning. Dkt. 94-1 at 65; Dkt. 94-2 at 42. Micron contends the term is indefinite because the term is supposedly susceptible to two different meanings. *See* Ex. 5 (Stone Decl.), ¶¶ 46-49. Courts have expressly rejected that approach. The test for indefiniteness is whether the claims inform a POSITA "about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 908-910 (2014) (declining to adopt a test rendering a patent invalid "when a claim is 'ambiguous, such that readers ***could reasonably interpret the claim's scope differently***'"). In other words, "[t]he test is not merely whether a claim is susceptible to differing interpretations." *Nevro Corp. v. Boston Sci. Corp.*, 955 F.3d 35, 41 (Fed. Cir. 2020). Micron's argument lacks merit.

A "strobe signal" is generally a signal that indicates that another signal, e.g., data, is present and valid, and can be used to accurately time the transmission of data throughout the module. Ex. 18 at 318 n.1; Ex. 4, 78:20-23 (Dr. Stone explaining that "[t]he data is timed to start appearing after the strobe"). The specification teaches that in DDR SDRAM—the prevalent memory technology at the time of the invention—"memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval," for example, as depicted in Fig. 6A. Ex. 2 ('215), 11:38-57.

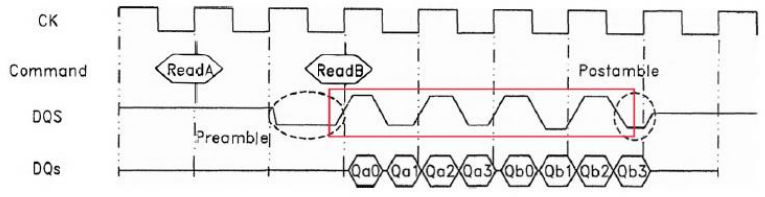


FIG. 6A

Ex. 26 ('215 patent, Ex. 12 to Stone Depo.) at 18.

Micron's expert opines that that "burst of data strobe signals" could mean a set of consecutively transmitted strobe signals originating from (1) two different memory devices with their strobe pins tied together ("combined strobe") or (2) a single memory device ("non-combined strobe"). *Id.*, ¶¶ 48-49. But Dr. Stone's emphasis on the origin of the "burst of data strobe signals" is misplaced: the claims can properly include both "types" of strobe signals. Indeed, Dr. Stone does not contend that a POSITA would not be able to identify any of the "burst of data strobe signals" in Figs. 7 and 19 of the '215 patent. *Id.* To the contrary, at deposition, Dr. Stone agreed that what is labelled in the red box above in Fig. 6A is a "series of data strobes:"

> Q. And you see what I've drawn here in this red box?
> A. I -- I have to -- I'm looking at my own copy. So let me know -- see what we're looking at. Is it on the screen?
> Q. Yes.
> A. I have to bring that up. Okay. I got it. I see a red box.
> Q. This is a series of data strobes; is that correct?
> A That's correct.

Ex. 4, 81:6-16; 82:4-7 (marking Ex. 12). The specification also makes clear that the claims cover both combined and non-combined strobe signals. For example, Fig. 7 of the '417 patent shows three different data strobe signal lines—one for strobe a, one for strobe b, and one for combined strobe. A POSITA would understand that the term "burst of data strobes" is correctly applied to each of those signal lines using the same meaning—expressly as shown in Fig. 7.

IX. "operable in a computer system to communicate data" ('215, claim 1; '417, claim 1)

Defendants argue this term should be construed to mean "configured in a computer system to communicate data." During meet and confer, the sole basis Defendants provided for replacing "operable" with "configured" was this Court's decision in T*Q Delta, LLC v. CommScope Holding Co., Inc.*, 2022 WL 2071073 (E.D. Tex. June 8, 2022), where, in the context of different patents, the Court construed "operable" as "configured." *Id.* at *9-10. Tellingly, neither Micron nor Samsung explained what it meant for a memory module to be "configured" in a computer system to communicate data,

e.g., whether under their construction the device has to be taken out of the box and configured by end users to infringe. *Id.* at *10 (emphasizing that "[a]t the June 1, 2022 hearing, Defendants stated that they will ***not*** argue that Plaintiff must prove that the accused devices are taken out of their packaging, plugged in, and turned on"). Defendants' nebulous construction should be rejected.

The claims differentiate between "operable" on the one hand and "configured" on the other hand. For example, claim 1 of the '215 patent uses "operable" in describing the communication between the memory module and the computer system, and "configured" when describing certain attribute of the memory module:

> 1. A memory module **operable in** a computer system . . . , the memory module comprising:
>
> a printed circuit board having a plurality of edge connections **configured to** be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
>
> a register coupled to the printed circuit board and **configured to** receive and buffer first command and address signals . . . ;
>
> logic coupled to the buffer and **configured to** respond . . . .

Ex. 2 ('215), 37:13-62. Claim 1 of the '417 patent likewise distinguishes between "operable" and "configured." *Compare* Ex. 3 ('417), 42:7, *with* 42:14, 51. The inventors clearly knew how to draft claims requiring memory modules to be "configured" in a particular way. "Different claim terms are presumed to have different meanings." *Bd. Of Regents of the Univ. of Tex. Sys. v. BENQ Am. Corp.*, 533 F.3d 1362, 1371 (Fed. Cir. 2008) (citations omitted). Neither Samsung nor Micron have provided any justification to depart from this principle and redraft "operable" to mean "configured."

TQ Delta is inapposite. In that case, the concern was whether the plaintiff's construction of "operable" was overbroad because it potentially encompassed scenarios where the claimed functionality required modification by the accused infringer. 2022 WL 2071073 at *9 ("Plaintiff's proposals of 'capable' and 'capable to' are therefore potentially overbroad because 'capable' might be

interpreted broadly as allowing for an ability that arises after modification."). That concern is not present here. A POSITA would understand that memory modules are designed to communicate data with a memory controller of the computer system via a memory bus without modifications. *See., e.g.*, Ex. 2 ('215), 1:49-53 ("[M]emory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system."); 5:18-21 (Fig. 1 illustrating that "memory module **10** is connectable to a memory controller **20** of a computer system"); 7:5-13 (Fig. 2 illustrating that "[t]he common DQ line 112 and the common DQS line 114 are electrically coupled to the memory controller 20 of the computer system"). Micron's expert also acknowledges this. Ex. 5 (Stone Decl.), ¶ 24 ("A computer basically consists of an instruction processing unit, ***which obtains instructions and data from a computer memory*** . . . ."); *id.*, ¶ 21. Dr. Stone further testified that "the modules in these patents are directed to modules that can -- are -- are in computer systems and can interact with the computer system." Ex. 4, 33:12-19. Thus, there is no ambiguity regarding what "operable" means in the context of the '215 and '417 patents, and Defendants' attempt to redraft the claims should be rejected.

X. "data buffer control signals" ('417, claims 1, 3, 11)

As with Samsung's proposed constructions for "logic" and "circuitry" (sections V.B and VI.B), Samsung here again attempts to import an additional 50+ words into the plain language of the claim. *See* Dkt. 94-2 at 12-13. This would exclude preferred embodiments, such as Figs. 8A and 8B. Thus, for the same reasons as above, Samsung's construction should be rejected. *Supra*, 18-20.

XI. "overall CAS latency" / "actual operational CAS latency" ('417, claim 1; '215 claims 3, 4, 24, 25)

Netlist and Samsung agree that these terms should be interpreted according to their plain and ordinary meaning. Micron, relying solely on extrinsic evidence, seeks to construe "overall CAS latency of the memory module" to mean "the delay between: (1) the time when **a *read command*** is executed

by the memory module, and (2) the time when the first piece of data is made available at an output of the memory module." *See* Ex. 5, ¶¶ 43-45 (relying solely on extrinsic evidence). Micron's construction of "overall CAS latency of the memory module" would improperly narrow the term to encompass read commands only, as would Micron's construction of the "actual operational CAS latency" terms.

First, the language of the claims supports constructions that include both read and write commands. Claim 1 of the '417 patent is expressly directed to both "read or write memory commands" and further states that "data ***transfers*** through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices." Ex. 3 ('417), 42:9-11, 42:63-37. Similarly, claim 1 of the '215 patent is directed to first memory command and second memory commands that respectively "cause the memory module to *receive or output* a [first or second] data burst." Ex. 2 ('215), 37:16-22.

Second, the specifications of the '215 and '417 patents support Netlist's constructions including both read and write commands. For example, the specification teaches that "[t]he one-cycle time delay of certain such embodiments provides sufficient time for read ***and write data transfers*** to provide the functions of the data path multiplexer/***demultiplexer***." Ex. 2 ('215), 20:39-42; Ex. 3 ('417), 22:53-56. Dr. Stone admitted that this passage indicates that CAS latency relates to read or write commands. Ex. 4, 76:16-18 ("Q. This passage is indicating that CAS latency can relate to both read and write data transfers? A. That's correct."). The specification also describes "data transfers ***between*** the memory controller and the memory module," and not just transfers ***from*** the memory module to the memory controller. Ex. 2 ('215), 20:27-29; Ex. 3 ('417), 22:41-43; *see also* Verilog code (both read and write). A POSITA would understand the "between" language, which specifies bidirectional data transfers, as referring to both read and write commands. Micron's proposals exclude these disclosed embodiments and should therefore be rejected. *Kaufman*, 34 F.4th at 1372 (a claim construction that excludes preferred embodiments is "rarely, if ever, correct").

Finally, Micron attempts to narrow these terms without demonstrating a clear disavowal of claim scope. Micron's expert relies exclusively on the DDR standards to argue that the disputed CAS latency terms must exclude write operations. Ex. 5 (Stone Decl.), ¶¶ 43-45. This is inappropriate because the claims recite "*overall* CAS latency" and "*actual operational* CAS latency," terms that are used and explained in the '215 and '417 patents, but not defined by the JEDEC standards. Furthermore, the DDR2 standard, which is repeatedly referenced in the '215 and '417 patent specifications, actually undermines Micron's construction of the disputed CAS latency terms. For example, in the DDR2 standard, both the read latency (RL) and the write latency (WL) depend on the CAS latency (CL) as well as AL. Ex. 8 (JESD79-2) at 24 (defining the following relationship: WL = RL - 1 = AL + CL – 1). In IPR, Micron admits that CAS latencies defined in the DDR2 standard JESD79-2 are for read and write commands. *See* Ex. 27 (Petition, IPR2023-01142) at p. 20 ("JESD79-2 also describes CAS latencies and adding additional clock cycles of latency when executing read and write commands."). Thus, even the cited standards do not support Micron's narrow construction.

Micron also contends that the term "wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices" in '417 claim 1 is indefinite. Dkt. 94-3 at 67-68. Micron's indefiniteness argument is apparently premised on its incorrect construction of the "CAS latency" terms, and should be rejected. Micron's expert offered no opinion as to whether this term is indefinite. *See generally* Ex. 5. Moreover, as discussed above, a POSITA would have no difficulty understanding the terms "overall CAS latency" and "actual operational CAS latency." *Supra*, 29-30. Nor is it a mixed method-apparatus term. *See Gesture Tech. Partners, LLC v. Huawei Device Co.*, 2021 WL 4760632, at *23 (E.D. Tex. Oct. 12, 2021) (claim not indefinite as mixed method-apparatus claim where "[t]he disputed term relates to configuration of the recited first camera rather than, for example, any user action or any action performed by or on the camera").

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that a copy of the foregoing document was served on Samsung's counsel through the Court's CM/ECF system on August 24, 2023.

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